VERSION OF SPECIFICATION WITH MARKINGS TO SHOW CHANGES MADE

Please replace Paragraph **[0001]** with the following:

[0001] This application is a continuation of application Serial No. 09/651,394, filed August 29, 2000, pending, which is a continuation of U.S. Patent Application Serial No. 08/844,669 filed April 18, 1997, now U.S. Patent [6,165,813]6,165,815, issued December 26, 2000, which is a continuation of U.S. Patent Application Serial No. 08/650,429, filed May 20, 1996, abandoned.

VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A method of fabricating a multi-level stack of semiconductor substrate elements, each of said elements including integrated circuitry, comprising:

providing a first semiconductor substrate element having a first side including integrated circuitry thereon and having a back side;

providing at least one second semiconductor substrate element having a first side including a plurality of integrated circuitry thereon and having a backside;

stacking said first semiconductor element and said at least one second semiconductor substrate element in a superimposed relationship having the back side of the first semiconductor substrate element facing the back side of the at least one second semiconductor substrate element aligning vertically said first semiconductor substrate element and the at least one second semiconductor substrate element to vertically align integrated circuitry on said first semiconductor substrate element and at least one of the plurality of integrated circuits on said at least one second semiconductor substrate element[;] and severing from said stack traversely at least one dice pair comprising a die from said first semiconductor substrate element and an aligned second die from said at least one second semiconductor substrate element; and

adhesively attaching said first semiconductor substrate element and said at least one second semiconductor substrate element.

4. (Amended) The method of claim 1, wherein said first semiconductor substrate element and at least one second semiconductor substrate element, each element including locations defining discrete dice or wafer portions severable from a first semiconductor substrate wafer and at least one second substrate wafer.

5. (Amended) The method of claim 1, wherein said first semiconductor substrate element and [the]said at least one second semiconductor substrate element each include a flat, and said vertical alignment is effected by aligning said flat of said first semiconductor substrate element and said flat of the at least one second semiconductor substrate element.

10. (Amended) The method of claim [1]9, wherein said intermediate connection elements are selected from a group consisting of bond wires and traces of flex circuits.

11. (Amended) The method of claim 10, further comprising:

connecting said at least one dice pair to conductors of [a]said substrate and encapsulating said at least one dice pair thereafter.

12. (Amended) A method of fabricating a multi-level stack of semiconductor wafer segments, each of said semiconductor wafer segments including integrated circuitry, comprising:

providing a first semiconductor substrate segment having a first side including integrated circuitry thereon and having a back side;

providing at least one second semiconductor substrate segment having a first side including a plurality of integrated circuits thereon and having a backside;

stacking said first semiconductor substrate segment and said at least one second semiconductor substrate [wafer]segment in at least partially superimposed relationship to form a stack of semiconductor wafer [segment]segments;

separating said stack to form at least two semiconductor wafer segment stacks, each said semiconductor wafer segment stack comprising a first semiconductor wafer segment having a side including integrated circuitry and a back side and at least one second semiconductor wafer segment having a side including integrated circuitry and a back side,

stacking said at least two semiconductor wafer segment stacks in at least partially superimposed relationship;

locating bond pads on said first semiconductor wafer segment of at least one of said at least two semiconductor wafer segment stacks on [the]a side adjacent said at least one second semiconductor wafer segment of said at least one semiconductor wafer segment stack at a periphery thereof;

forming a notch through said at least one second semiconductor wafer segment of said at least one semiconductor wafer segment stack, said notch extending between and substantially perpendicular to a circuitry side and a back side of said at least one second semiconductor wafer segment to provide access to at least one said peripheral bond pad of said first semiconductor wafer segment of said at least one semiconductor wafer segment stack; and

adhesively attaching said first and said at least one second semiconductor wafer segments of said at least one semiconductor wafer segment stack.

18. (Amended) A method of fabricating a multi-level stack of semiconductor wafers, each of said semiconductor wafers including integrated circuitry, comprising:

providing a first semiconductor wafer having a first side including integrated circuitry and having a back side;

providing at least one other semiconductor wafer having a first side including integrated circuitry and having a back side;

stacking said first semiconductor wafer and said at least one other semiconductor wafer in a superimposed relationship;

locating bond pads on said first semiconductor wafer of said stack on [the]a side proximate said at least one other semiconductor wafer at a periphery thereof;

forming a notch through said at least one other semiconductor wafer, said notch substantially perpendicular to a circuitry side and [a]the back side of said at least one other semiconductor wafer providing access to at least one said peripheral bond pads of said first semiconductor wafer of said stack; and

adhesively attaching said first semiconductor wafer and said at least one other semiconductor wafer.

19. (Amended) The method of claim 18, further including:

stacking said first semiconductor wafer and said at least one other semiconductor wafer with a third semiconductor wafer, having the integrated circuitry side of said first semiconductor wafer segment proximate [the]said back side of said third semiconductor wafer.